Research Infrastructure Overview

Anil Kottantharayil
Associate Professor
Department of Electrical Engineering and Centre of Excellence in Nanoelectronics, IIT Bombay, Powai, Mumbai -76, India.

E-mail: anilkg@ee.iitb.ac.in
Executive Summary

• Activities in all aspects of nanoelectronic device physics, technology, characterization, TCAD, modeling and VLSI design
• 41 faculty members, 70 Ph. D. students and 60 M. Tech & DD students from 8 departments across the institute use the facility
• CEN is a national facility being used by 67 entities, including industry users
• Total funding to the tune of 150 cr. in the last 6 years
• Applied Materials Inc. (AMAT) donated equipment ~ 41 cr.
• Funding in the pipeline ~ 95 cr.
• Total lab space of 35000 sq. ft.
• Facilities in the institute on high performance computing and materials characterization (SAIF, and Central facilities)
Fabrication facility
Fabrication facility (2)
Fabrication facility (3)

• 41 pieces of high end fabrication equipment
  • thin film growth & deposition (oxidation, CVD, sputter,....)
  • lithography (optical aligner, direct laser writer, e-beam)
  • reactive ion etch
  • doping (diffusion and PIII)
  • wet processes
• 11 pieces of material characterization equipment
  • scanning probe microscopes
  • optical microscopes
  • SEM
  • spectrometers, ellipsometer, ..... 
• 11 more fabrication equipment in the pipeline (MBE, glove boxes...)
• 8 more material characterization equipment in the pipeline (XRD, XPS, XRR, PL, ..... )
Electrical Characterization

40 GHz, 4 Probe SUSS Microtec pm5

Semiconductor parametric measurement system
Electrical Characterization (2)

• Parametric and low frequency device characterization
  • Parametric IV & CV measurement systems – 7
  • Low frequency noise, charge pumping
  • Device reliability tests like HCE, NBTI, dielectric wear out
• Analog, Mixed-Signal and RF IC/System Test
  • 40 GHz, 4 Probe SUSS Microtec pm5
  • Network analyzer (40 GHz), Signal generator (6 GHz), DSO (2 GHz), Spectrum analyzer (6 GHz)
• 5 more electrical characterization equipment in the pipeline (cryo probe station, transient high speed opto-electronic measurement system, ....)
Computational Nanoelectronics

• Microelectronics Computation Lab
  – 25 state-of-the-art Xeon/Opteron workstations
  – Sentaurus TCAD (process & device modeling: 25 licenses for R&D + education)
  – Materials Studio (materials modeling)
  – COMSOL (multiphysics)
  – MEMS (Coventor ware, Intellisuite)

• EE Department Labs
  – MATLAB (numerical computing platform)

• IITB HPC Cluster “Space-Time”
  – Several materials modeling tools

• Proposal for Computational Nano Centre in concept stage
VLSI Design Lab

• Design Environments (Complete Flow)
  • Cadence Virtuso Custome IC Design Flow (Analog/Mixed-Signal/RF Design, Simulation and Layout and Verification Environment)
  • MentorGraphics ICflow 2006.1
• Logic Synthesis Tools (ASIC)
  • Cadence Encounter
  • Synopsys Design Compiler
• Hardware Accelerator
  • IMAGE Hardware Emulator - IMAGE, Powailabs
Indian Nanoelectronics Users’ Program (INUP)

• INUP is a vehicle for making the CEN facilities available to researchers from other academic institutions, R&D laboratories and industry

• Manpower training in nanoelectronics beyond IIT-B and IISc
  – Disseminate knowledge in nanoelectronics
  – Generate wide-spread “hands-on” expertise by short term hands-on workshops and enabling execution of research projects

• A well considered IP policy is in place

• A pool of expertise in nanoelectronics for sponsored/collaborative research and consultancy
## INUP: 3 year Status Summary

<table>
<thead>
<tr>
<th>Category</th>
<th>Medium term projects (3 to 24 months)</th>
<th>Short term projects (&lt; 3 months)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Completed</td>
<td>9</td>
<td>13</td>
</tr>
<tr>
<td>On-going/approved</td>
<td>26</td>
<td>26</td>
</tr>
<tr>
<td>Total # of projects</td>
<td>35</td>
<td>39</td>
</tr>
<tr>
<td>Total number of published papers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Journal</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td>Conference proceedings/presentations</td>
<td>42</td>
<td></td>
</tr>
<tr>
<td>Number of patents filed</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Number of Ph. D. thesis</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Number of M. Tech/M. Phil thesis</td>
<td>19</td>
<td></td>
</tr>
<tr>
<td>Manpower trained</td>
<td>L1 (424), L2 (136), L3 (114)</td>
<td></td>
</tr>
<tr>
<td>Familiarization workshops</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Hands-on training workshops</td>
<td>6</td>
<td></td>
</tr>
</tbody>
</table>
**Capacity:** 5 to 100 million gate

**Acceleration:** From 100X to 1000X acceleration over pure simulation for [Verilog, VHDL, mixed] language designs.