Centre of Excellence in Nanoelectronics

V. Ramgopal Rao
Indian Institute of Technology, Bombay

Picture above & Phase-2 slides courtesy: Prof. Rudra Pratap IITSc
Presentation Outline

- Brief background
- Phase I Achievements (2006-2011)
- Phase II (Jan 2012)
  - Research plan
  - Education & HRD
  - Application development & commercialization
  - Incubation
Establishment of CENs at IITB & IISc is a watershed event in Indian academic research. It addresses three most significant problems of Indian scientific research effort:

- Poor connection between science and technology
- Overemphasis on theory and much less effort on experiments
- The gaping hole between research and commercialization
CENs’ Foundational USPs

• Unique project in scope, objectives, infrastructure, and outreach
• “Grass-roots” initiative; not driven by a singular big personality
• Clear short term, medium term, and long term goals
• Driven by a genuine desire to make social impact
Investigators at IITB (1)

Faculty involved: 40

- EE
- Mat. Sci
- Phys.
- Chem.
- Bio.
- Rel.
- Mech.
- Energy

IIT Bombay
Funding Raised

- Centre of Excellence in Nanoelectronics (CEN) in 2006 (US $12 M)
- Applied Materials funded the AMAT Nanofabrication Lab in 2007 & other sponsored projects (~US$ 10 M)
- Indian Nanoelectronics Users Program created in 2008 (US$ 2.5 M)
- ISRO/DRDO/Other Govt. agencies (2007-2011) (~US $ 20 M)
- National Centre for Photovoltaic Research & Education (NCPRE) (MNRE) (US $ 10 M)
- Industry Sponsored Projects (2006-2011) (US $ 1.5 M)
Now a Rs. 200 crore facility
24x7 operation
Used by over 200 researchers from over 60 institutions
IITB: CEN Research Areas

• 5 important “Areas”
  – Sub-100 nm CMOS Process Development
  – Nanosystems for Healthcare and Environmental Monitoring
  – Organic & Biopolymer Devices
  – GaN Devices
  – Characterization, Modeling and Simulation of Nanoelectronic Devices

• 1 “Joint Deliverable” together with IISc
  – RF Oscillator with on-chip LC resonator and sub-100 nm transistors

• Other activities in addition to the above research areas
#1: Sub 100 nm CMOS Process Development
(Anil KG., Swaroop Ganguly, P. R. Apte, R. Pinto, J.Vasi, V.Ramgopal Rao)

Timelines:

✓ 0-1.5 Year : Setting up the facility
✓ 1-2.5 Year : Unit Process Development and Optimization
✓ 2-4 Year : Process Integration and Optimization

Equipment:
✓ Electron Beam Lithography System
✓ Optical Mask Aligner with sub-micron resolution
✓ Two Chamber RIE System for Metals and Polysilicon (part of AMAT donation)
✓ ALD System for High-K Materials (part of AMAT donation)
✓ ALD/CVD systems for SiGe (part of AMAT donation)
✓ 3 stack furnaces (2X)
✓ 4 stack LPCVD furnace
✓ Other miscellaneous processing equipment
Deliverable #1: sub-100nm transistor

1. Lithography
   500nm $L_{\text{poly}}$ (100nm $\rightarrow$ direct-writing)
   Active area on mask

2. LOCOS
   Field oxide: ‘bird’s beak’

3. Gate stack
   Anisotropic poly etch

4. Spacers
   Very selective nitride-to-oxide etch

5. Silicided S/D
   NiSi ‘source/drain’

- All unit processes, most modules are in place for sub-100nm transistor
- Sub-micron transistor fabrication is in progress now
- Interaction with IISc has been initiated for oscillator integration
- Interaction with a PV start-up initiated for Si process development @ CEN
Nanoscale logic and memory technology: products with “IITB inside”

**STBFET**

- SS < 20 mV/dec with a significantly higher $I_{ON}$
- US Patent filed jointly with Infineon

**A Novel Junction-less Transistor**

- Scalable to 10 nm Gate lengths

**Si QD based solar cells**

**Metal nano-crystal Flash memory**

Various Nano-scale CMOS devices to be pursued as part of Phase II activities
#2: Nanosystems for Healthcare and Environmental Monitoring

Timeline:
- 0 – 1.5 Year: Setting up of systems
- 0 – 2.5 Year: Standardization of unit processes
- 1 – 3.5 Year: Integration of processes for microfabricated structures
- 2 – 4.5 Year: System integration and tests
  - 3 – 5 Year: Documentation

Equipment needed:
- Electron Beam Lithography System
- Double sided Mask Aligner & Wafer Bonder
- Two Chamber RIE System for Metals and Polysilicon (AMAT donation)
- 3 stack furnaces (2X)
- 4 stack LPCVD furnace
- other miscellaneous processing equipment
- PCR/SPR

To be pursued as part of Phase II activities - applications & further technology upgradation
A company “NanoSniff Technologies Pvt. Ltd.” is incubated at IIT Bombay based on this technology. Rs. 4 crore private investment raised and there are 13 people currently working in the company including 4 Ph.Ds.
iSens Bio-Chip

Specifications:

- Base material: Poly-di-methyl-siloxane (PDMS) elastomer
- Fabrication: Simple MEMS fabrication processes (optical Lithography, Plasma treatment, etc.)
- Volume: 10-20 µL
- Advantages: Biocompatible, easily patternable, surface-modification easy, transparent
A polymer composite cantilever based iSens Prototype for cardiac Diagnostics
Ver-2: iSens
Working prototype
Silicon Locket

- Low power ASIC based – Fabricated & working fine
- Low cost SU8 Accelerometer – Motion artifacts
- Undergoing field trials in hospitals
- TCS-Industry partner

Lead investigator: Prof. D.K. Sharma & colleagues from Bio-school
A miniaturized 3 channel 12 lead ECG unit

- This extremely small ECG unit can take data on three channels simultaneously.
- Electrodes can be attached to any three of the 12 standards leads.
- It uses a flexible “platform” technology to provide a choice of analog front ends and a choice of communications protocols.
Polymer Composite Microaccelerometer

Seena et al., IEEE/ASME Journal of MEMS, 2011
### #3: Organic and Biopolymer Devices

(A. Q. Contractor, Anil Kumar, V. Ramgopal Rao, S. Mukherji, D.K. Sharma, R. B. Sunoj)

#### Timeline:
- **0 - 1 Year:** Design and fabrication of suitable set-up’s for deposition of conjugated polymer on microelectrodes.
- **0 - 1 Year:** Design and fabrication of microelectrodes.
- **0 - 2 Year:** Standardization of protocols for polymerization.
- **0 - 5 Year:** Electrical characterization of devices.
- **1 - 5 Year:** Incorporation of biomolecules into the polymer matrix.
- **1 - 5 Year:** Measurement of electrical and sensor characteristics of the devices.
- **2 - 5 Year:** Integration of devices with silicon devices.

#### Equipment needed:
- Potentiostat.

Again, applications to be pursued as part of Phase II activities.
Functional Conducting Polymers

3,4-propylenedioxythiophene

Syntheses

Electrochromics

Nano-Structures

Sensors

Electronic Tongue

3,4-propylenedioxysilole

Printable Electronics

Transparent Conductor

Electrochemcal Transistors

Immunno DNA

Nerve Agents

Electronic Nose

Fluorescence Quenching

Explosives

Biosensors

Thin Film Transistors

Radiation
First Generation Handheld Device for detection of TNT and RDX at Room Temperature

- Sub ppt sensitivity
- Highly selective
- 50 prototypes
- Available for field trials
World’s most sensitive Polymer Composite cantilever Platform

V Seena et al., “Polymer nanocomposite nanomechanical cantilever sensors: material characterization, device development and application in explosive vapour detection,” Nanotechnology, 22 (2011)(11pp) (top 10 most downloaded articles)
Explosive Detector Prototype for RDX/TNT developed @ IIT Bombay

Seena et al., *IOP Nanotechnology*, 22 (2011) 295501
## HEMRL test report for the Cantilever sensors developed at IIT Bombay

- **D** = Detected; **ND** = Not Detected

<table>
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<th>Cantilever based system with proprietary surface coatings</th>
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<td>HMX</td>
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<tr>
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</table>
Miniaturized wireless explosive detector

Packaged flow cell for explosive detection

Fully automated and stand off detection

PCBs for wireless explosive detector
Piezoelectric Cantilevers

- Energy Scavenging from vibrations
- *Self powered wireless Explosive Sensor Networks*

![Graph showing frequency vs. voltage](image)

![Diagram of cantilever structure](image)

![Image of wireless explosive detector](image)
# 4: GaN Devices
(D.Saha, S.Chakraborty, S.Ganguly, S.Dhar, J.Vasi, B.M.Arora, R.Pinto (close collaboration with TIFR))

Timeline:

- Year 1: GaN material growth on sapphire substrate (TIFR system)
- Year 2: p-GaN material growth on sapphire, GaN growth on (100) and (111) silicon
- Year 3: Ohmic contact for GaN, Schottky diode development
- Year 4: Diode characterization, Nanoscale GaN patterning for nanowires, nanodots
- Year 5: Nanoscale GaN device fabrication and characterization (electrical, optical)

Equipment needed:
- GaN MOCVD (collaboration with TIFR/Anna University)
- Optical Mask Aligner with sub-micron resolution
- RIE System for GaN
- ALD System for High-K Materials (AMAT donation)
- 3 stack furnaces (2X)
- 4 stack LPCVD furnace
- other miscellaneous processing equipment

To be pursued as part of Phase II activities
GaIN Based HEMT

Device Schematic

Gate Schottky Contact

Ohmic Contact

Source/Drain ohmic Contact

Schottky Contact

Voltage, V (V)

Current, I (mA)

-20 -15 -10 -5 0 5 10 15 20

40

0

-10

-2 -1 0 1 2 3 4

Source

Drain

Gate

Sapphire Substrate

GaN (4 nm)

AlN (1.5 nm)

AlGaN (25 nm)

GaN (1 μm)

Device Micrograph
GaN Based HEMT

- **Peak transconductance**, $G_{m,\text{peak}} = 140 \text{ mS/mm}$

- **Threshold voltage**, $V_{\text{TH}} = -25 \text{ V}$

*Close interactions with SSPL*
#5: Characterization, Modeling and Simulation of Nanoelectronic Devices

(S. Mahapatra, M. B. Patil, J. Vasi, R. B. Sunoj, S. Ganguly, J. Vasi, Anil KG, V. Ramgopal Rao)

**General:**
- ✓ 0 – 1 Year: Equipment ordering & purchase
- ✓ 1/2 – 2 Year: Setup, calibration, standardization

**Reliability:**
- ✓ 1/2 – 2 Year: NBTI on nitrided gate oxides
- ✓ 1 – 3 Year: HCI and NBTI - HCI co-modeling
- ✓ 2 – 5 Year: TDDB, NBTI - HCI - TDDB co-modeling
- ✓ 1/2 – 4 Year: Reliability of SONOS flash & modeling
- ✓ 3 – 5 Year: Reliability of nano-particle flash & modeling

**Other characterization:**
- ✓ 2 – 5 Year: Detailed characterization when devices are available from 1 – 4.

**Modeling and simulation:**
- ✓ 0 – 1 Year: Ordering, installation of software packages, preliminary testing

**Equipment needed:**

- Prober x 2 (high-end), Prober x 1 (low-end), Matrix scanner x 4, d) Pulsed sources (x2 high-V, x5 low-V, x1 high-f), SMUs (x2 low current), A4155 parameter analyzer, Network analyzer, Logic analyzer, Sampling DSO, Test vector generator, Cryostat, Constellation analyzer, DLTS & PL setup, Device and process simulators (donation from Synopsis), Molecular simulator

To be pursued as part of Phase II activities
Status: Characterization

Close industrial interaction → industrially relevant problems

Example: CMOS device reliability

CEN-IITB as one of the top R&D center → Large no. of publications in top conferences & journals

JEDEC (Electronics Industry standards) refers measurement & modeling methodologies developed by researchers in CEN-IITB

Invited talks & invited tutorials (to industrial participants) by CEN-IITB researchers in several leading conferences in USA, Europe & Asia-Pacific
Indigenously Developed Hot-Wire CVD Cluster Tool/Plasma Implantation System

- Applied Materials integrated HWCVD into one of their PV tools
- % FE component reduced by ~25% in phase-2
Industry Collaborations

• Sponsored, Consultancy & Collaborative Projects
  - Indian industry: SCL, BEL, SITAR, TCS, Sasken, TII, Cypress, ControlNet, National, L&T, BIGTEC etc
  - International industry: Intel, Motorola, GE, Siemens, Hitachi, Renesas, TSMC, IME, Agere, IMEC, Applied Materials, IRC, Vishay, SRC, IBM, Maxim, Infineon

• Industry sponsorship of students
  - M.Tech. & Dual Degree students
  - Ph.D. students

• Endowed Laboratories
  - Gaitonde Integrated Systems Laboratory
  - TCS VLSI Design & Characterization Laboratory
  - Applied Materials Nano-manufacturing Laboratory

• Continuing Education Programs for industry

➢ Rs. 7 Crore funding from industry projects since 2006
Publications from CEN @ IIT Bombay
2006-2010

Journal Publications: 130
Conference Publications: 150
IEEE Journals (2006-2010): 70
International Electron Devices Meeting (IEDM): 9
International Reliability Physics Symposium: 10

<table>
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CEN: Industrial Interaction

- Equipment donation
- Sponsored projects
- Joint publication
- Joint patents
- Press coverage
- International visibility
Applied Materials Nanofabrication Facility

Gate Stack Centura  Etch Centura  PVD Endura

Applied Materials: Major semi-tool manufacturer
Equipment donated, value USD 7.5M
Manned jointly by AMAT & IIT-B staffs
Further tool donation for PV activities (2010)
Some Ongoing Sponsored Projects

**Applied Materials, USA:** Charge trap memory based on silicon nitride, metal nanodot memory, reliability of SiON and HiK MOSFET devices, solar cells, polymers, Low-k dielectrics, Ge Path finding project

**Intel, USA:** Simulator development for metal nanodot memory, mixed signal CMOS, Multi-gate device-circuit co-design

**Infineon, Germany:** I/O circuit applications, ultra low-power CMOS, sub 22nm technology/ device options

**L&T, India:** MEMS switches for power electronics

**TI, India:** Rad-hard CMOS for space application
Some Ongoing Sponsored Projects

**BARC, India:** Radiation Sensors

**IBM, USA:** Technology-design issues involving multi-gate FETs

**TSMC, Taiwan:** Split Gate Flash Memory device

**Micron, USA:** Vertical MOSFET for RRAM applications

**Renesas, Japan:** SiON and Hi-K MOSFET reliability

**Hitachi, Japan:** SONOS memory

**SRC, USA:** Charge trap memory, Hi-k dielectrics for logic devices
Joint publications

Joint publications with Industry in major international conferences (IEEE-IEDM*, IEEE-IRPS*) and journals (IEEE-TED, EDL)

*CEN the only Indian entity ever presented in these prestigious conferences

Example (2006-2009):

IITB-AMAT: IEDM (5), IRPS (4), TED/EDL (10)

IITB-Infineon: IEDM (3), IRPS (5), TED/EDL (14)
On the Physical Mechanism of NBTI in Silicon Oxynitride p-MOSFETs: Can Differences in Insulator Processing Conditions Resolve the Interface Trap Generation versus Hole Trapping Controversy?

S. Mahapatra¹#, K. Ahmed², D. Varghese¹, A. E. Islam³, G. Gupta¹, L. Madhav¹, D. Saha¹ and M. A. Alam³

¹Department of Electrical Engineering, IIT Bombay, Mumbai 400076, India (*)Email: souvik@ee.iitb.ac.in
²Applied Materials, Santa Clara, CA; ³School of EECS, Purdue University, W. Lafayette, IN

ABSTRACT

Negative Bias Temperature Instability (NBTI) is studied in plasma (PNO) and thermal (TNO) Si-oxynitride devices having varying EOT. Threshold voltage shift ($\Delta V_T$) and its field (EoX), temperature (T) and time (t) dependencies obtained from no-delay on-the-fly linear drain current ($I_{DLIN}$) measurements are carefully compared to that obtained from Charge Pumping (CP). It is shown that thin and thick PNO and thin TNO devices show very similar NBTI behavior, which can primarily be attributed to generation of interface traps ($\Delta N_{IT}$). Thicker TNO devices show different NBTI behavior, and can be attributed to additional contribution from hole trapping ($\Delta N_h$) in pre-existing bulk traps. A physics based model is developed to analyze and explain the EOT dependence of NBTI in PNO and TNO devices.

EXPERIMENTAL DETAILS

Experiments were performed on PNO and TNO devices having varying EOT (12Å through 22Å) and varying $N_2$ dose (up to 21% for thin EOT, up to 29% for thick EOT). On-the-fly
A NEW PHYSICAL INSIGHT AND 3D DEVICE MODELING OF STI TYPE DENMOS DEVICE FAILURE UNDER ESD CONDITIONS

Mayank Shrivastava¹, Jens Schneider², Maryam Shojaei Baghini³, Harald Gossner², V. Ramgopal Rao¹

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Mumbai-400076, India, mailto:mayank@ee.iitb.ac.in; mailto:rrao@ee.iitb.ac.in
²Infineon Technology AG, P.O. Box 80 09 49, D-81669 Munich, Germany, mailto:Harald.Gossner@infineon.com

Abstract

We present experimental and simulation studies of STI type DeNMOs devices under ESD conditions. The impact of base-push-out, power dissipation because of space charge build-up and, regenerative NPN action, on the various phases of filamentation and the final thermal runaway is discussed. A modification of the device layout is proposed to achieve an improvement (~2X) in failure threshold (I_{TH}).

I. INTRODUCTION

Aggressive scaling has resulted CMOS devices operating below 1 volt in sub 100nm node technologies. To communicate with were only through 2D simulation, and the 3D filament behavior was not clear. Also the proposed regenerative NPN action in the device was discussed for CDM time domain (1-2ns), whereas the device does not get heated within this short interval of time. These simulation studies also show influence in saturation drift velocity at temperatures higher than 1000 °K, which itself is sufficient for the onset of filamentation because of NDR and further thermal runaway. The study does not also discuss about base-push-out behavior. Other studies show that because of space charge limited current, peak electric field shifts at drain contact which causes regenerative avalanche injection. This again leads to filamentation and device failure [7][8]. A more detailed 3D modeling of filamentation has shown that regenerative turn on of parasitic NPN causes short circuit power dissipation and leads to
Press coverage

IIT-Bombay, Applied Materials and SRC Collaborate to Advance Flash Memory Technology

May 19, 2008 10:15 AM US Eastern Timezone

The Semiconductor Research Corporation (SRC), through its Global Research Collaboration program, announced a collaborative effort between the Indian Institute of Technology at Bombay (IIT) and Applied Materials, Inc. to advance NAND flash memory technology.

An example of this important research has recently been presented by IIT and Applied Materials at the recent International Reliability Physics Symposium in Phoenix, AZ. As NAND flash devices continue to scale, problems with reliability and lifetime caused by cell-to-cell interference arise when conventional floating-gate (FG) memory cells are used. Charge-trap flash (CTF) is a promising replacement for FG because it exhibits negligible cell-cell interference, yet has a similar structure and manufacturing process to FG and is thus attractive for memory device manufacturers to implement using existing equipment.

The primary innovation is the development and optimization of an engineered trap layer consisting of two nitride layers with different compositions, reinforced by a silicon oxy-nitride barrier layer. This novel structure was found to exhibit negligible cycling degradation and optimum programming characteristics, offering an alternative to approaches using more complex high-k and metal gate materials. The new structure has the potential to scale down to the sub-3xnm technology node, offering much higher storage densities than are available today.
Infineon, Indian researchers claim ESD advance

K.C. Krishnadas
(05/21/2009 11:29 AM EDT)
URL: http://www.eetimes.eu/germany/217600450

A joint research team from Infineon Technologies and the Indian Institute of Technology, Bombay, is claiming an advance in the integration of high-voltage functionality for advanced CMOS technologies.

BANGALORE, India — A joint research team from Infineon Technologies and the Indian Institute of Technology, Bombay, is claiming an advance in the integration of high-voltage functionality for advanced CMOS technologies.
IEDM Confronts Logic Scaling Challenges

The International Electron Devices Meeting (IEDM), set for Dec. 6-9 in Baltimore, includes presentations on new annealing techniques, FinFETs, compound semiconductors and random telegraph noise. The conference, with 215 paper presentations, will be preceded by a Sunday short course on scaling challenges organized by TSMC’s Howard C.H. Wang.

David Lammers, News Editor -- Semiconductor International, 10/15/2009

While the 55th International Electron Devices Meeting (IEDM) takes a brief detour to Baltimore this year, the conference — arguably the premier event for semiconductor technologists — will maintain its focus on the challenges of device scaling.

An IEDM paper given by researchers from the Indian Institute of Technology-Bombay and Infineon Technologies will compare simulated results from planar and non-planar SOI devices. "Non-planar devices perform poorly in comparison to ultrathin body (UTB) planar SOI MOSFETs, and are not the ideal choice for SoC applications," the paper’s abstract concludes.
Infineon, IIT Bombay: Gains in HV for Advanced CMOS

Researchers from Infineon and IIT Bombay have since 2007 been collaborating to do advanced research in IO device design and multi-gate MOSFETs for sub-45nm CMOS. They recently announced "... a major breakthrough in integration of high voltage (HV) functionality for advanced CMOS technologies."
ESD keeps EDA tools hopping

By Nicolas Mokhoff

EDA DesignLine (05/26/2009 10:25 AM EDT)

A joint research team from Infineon Technologies and the Indian Institute of Technology, Bombay, is claiming an advance in the integration of high-voltage functionality for advanced CMOS technologies.

The joint program, launched in 2007, focuses on advanced research into the areas of I/O device design and multi-gate MOSFETs for sub-45-nm node CMOS technologies.

"The collaboration has been very helpful to us in understanding the complex nature of some of the existing device reliability issues, and the solutions proposed significantly improve our products," said Harald Gossner, senior principal engineer for ESD research at Infineon.

Related Companies
- Infineon Technologies

Related Content
TECH PAPER
1. Adaptability Breeds Success in IP Development
TECH PAPER
2. Combining Low Pin Count Test with Scan Compression Dramatically Reduces Test Interface and Cost
TECH PAPER
3. New Method for Power Integrity and EMI Design
IIT student wins award for revolutionary research

August 22nd, 2008

IIT student wins award for revolutionary research

Abstract:
Prashanthi Kovur, a PhD student from the Centre for Excellence in Nanoelectronics, EE Department, IIT Bombay has been awarded the outstanding student researcher in the field of Physics, Chemistry of Material for nano-scale devices by the world largest semiconductor company TSMC.

Taiwan Semiconductor Manufacturing Company (TSMC) is one of the world’s largest semiconductor foundry, which provides leading technologies for the semiconductor manufacturing industry. The purpose of the TSMC Outstanding Student Research Award is to recognize exceptional semiconductor related research carried out by graduate students. The competition for this award attracted hundreds of applications from students from various universities all over the world.

Source:
Le Monde


_Lors_ de sa visite en décembre dernier sur le campus de l'Institut indien de technologie (IIT) Bombay, l'une des plus prestigieuses écoles d'ingénieurs indiennes, le président russe Dmitri Medvedev s'est longuement arrêté devant un petit aspirateur de la taille d'une main. Ramgopal Rao, qui était à ses côtés ce jour-là, se souvient, non sans fierté, de l'émerveillement du chef d'État devant son invention.

Read the rest of the article (in French) by journalist Julien Bouissou on the Le Monde’s website, or a copy of it here:
Best Student Paper
awarded to
Sudip Nag
in recognition of

Nov 14, 2011
Dr. Rao R. Tummala
2011 GIT General Chair

Nov 14, 2011
Mr. Dean A. Sutter
2011 GIT Academic Session Chair

Won among over 50 submissions from all over the world...
Faculty before the initiation of the CEN Activity

Prof. P.R. Apte  Prof. A.N. Chandorkar  Prof. M.P. Desai  Prof. S. P. Duttagupta  Prof. Juzer Vasi  Prof. S. Mahapatra

Prof. H.Nararyanan  Prof. M.B.Patil  Prof. Richard Pinto  Prof. V. Ramgopal Rao  Prof. D.K.Sharma

12 faculty members (group is in existence since 1982)
New Faculty Recruits in EE because of CEN activity (since 2006)

- Prof. A. Kottantharayil, Ph.D. (joined from IMEC)
- Prof. A. Kumar, Ph.D. (UC, Berkeley)
- Prof. Maryam Shojaei Baghini, Ph.D. (Sharif University)
- Prof. Chetan S. Solanki, Ph.D. (IMEC, Belgium)
- Prof. A. Tulapurkar, Ph.D. (joined from Stanford)
- Prof. Subhananda Chakrabarti, Ph.D. (joined from Michigan)
- Prof. Saurabh Lodha, Joined from Intel, Portland
- Prof. Udayan Ganguly, Ph.D. (Cornell University)
- Prof. J. Mukherjee, Ph.D. (Ohio State University)
- Prof. Swaroop Ganguly, Ph.D. (U of Texas, Austin)
- Prof. Sholab Gupta, Ph.D. (UC, Los Angeles)
- Prof. Pradeep Nair, Ph.D. (Purdue)
- Prof. A. T. Tulapurkar, Ph.D.
- Prof. Saurabh Lodha, Joined from Intel, Portland
- Prof. Udayan Ganguly, Ph.D. (Cornell University)
- Pradeep Nair, Ph.D. (Purdue)

13 New Faculty in the Nanoelectronics area since 2006 + 3 adjunct faculty from industry
National Centre for PV Research & Education (NCPRE)

- Jawaharlal Nehru National Solar Mission (JNNSM) announced in November 2009
- The Mission document lists, among steps which may be required for human resource development:
  
  “Setting up of a National Centre for Photovoltaic Research and education at IIT Mumbai, drawing upon its Department of Energy Science and Engineering, and its Centre of Excellence in Nano-Electronics”

- CEN is invoked by name in the JNNSM document
- The existence of a full running silicon facility available at CEN led Dr. Chidambaram, PSA to Govt. of India to propose that the NCPRE be set up at IITB
<table>
<thead>
<tr>
<th>Physical achievements</th>
<th>1\textsuperscript{st} Year</th>
<th>2\textsuperscript{nd} Year</th>
<th>3\textsuperscript{rd} Year</th>
<th>3 Year status</th>
<th>5 Year Target</th>
</tr>
</thead>
<tbody>
<tr>
<td>INUP @ IIT Bombay</td>
<td>Target</td>
<td>Achieved</td>
<td>Target</td>
<td>Achieved</td>
<td>Target</td>
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<tr>
<td>Familiarization Workshops</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Trained Manpower</td>
<td>Level 1</td>
<td>50</td>
<td>142</td>
<td>50</td>
<td>78</td>
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<tr>
<td>Level 2</td>
<td>10</td>
<td>30</td>
<td>15</td>
<td>56</td>
<td>20</td>
</tr>
<tr>
<td>Level 3</td>
<td>4</td>
<td>10</td>
<td>6</td>
<td>62</td>
<td>10</td>
</tr>
<tr>
<td>Projects (Medium)</td>
<td>Accepted</td>
<td>2</td>
<td>15</td>
<td>3</td>
<td>20</td>
</tr>
<tr>
<td>Completed</td>
<td>-</td>
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<tr>
<td>Sr. No</td>
<td>Workshop</td>
<td>Date</td>
<td>Number of participants</td>
<td>In collaboration with</td>
<td></td>
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<tr>
<td>1</td>
<td>2\textsuperscript{nd} INUP Workshop on Nanofabrication Technologies</td>
<td>May 30-31, 2009</td>
<td>165</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>3\textsuperscript{rd} INUP Familiarization Workshop: 2\textsuperscript{nd} International Winter School for Graduate Students (IWSG)</td>
<td>November 30-December 12, 2009</td>
<td>78</td>
<td>Cornell University</td>
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<tr>
<td>3</td>
<td>4\textsuperscript{th} INUP Familiarization Workshop “International Winter School on Nano-scale Materials and Devices”</td>
<td>December 13 - 17, 2010</td>
<td>135</td>
<td>University of Cambridge, UK</td>
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<tr>
<td>4</td>
<td>5\textsuperscript{th} INUP Familiarization Workshop: Joint Indo Canadian Meeting on Development of Low Cost Lab-on-a-Chip Medical Devices for Health Monitoring</td>
<td>January 7-11, 2011</td>
<td>69</td>
<td>University of Alberta, Canada</td>
<td></td>
</tr>
</tbody>
</table>
Incubation activities

Indian patents = 10, US patents = 13
(Multiple patents are currently under different stages of filing)

NanoSniff Technologies Pvt. Ltd.
- including setting up a manufacturing plant for sensors required for building a low-cost cardiac diagnostic system & an explosive detection system. Rs. 4 crore private investment raised and there are 13 people currently working in the company including 4 Ph.Ds.
Phase II: A Natural Extension of CEN
Phase I

Phase I Major Achievements

• Internationally visible centres and establishment of world class nanofabrication facilities
• Cohesive and focused research goals
• Unprecedented manpower training and outreach (through INUP) in nanoelectronics
• Internationally visible research output
• Technology development and lab prototypes
Phase II: Broad Objectives

- H²Rg: High-tech Human Resource Generation
- R&P: Research & Productization
- N₂O: National Network for Outreach
- eFRS: Experimental Facilities with Round-the-clock Service
Phase II: Broad Objectives

A High-tech Eco System

- To support technology breakthroughs & completely new ideas
- To encourage start-ups and technology entrepreneurs
- To support High-tech industries
Project Deliverables
Deliverables

- Basic Research
- Technology Creation
- Commercialization
1. Novel MOSFET structure for sub-0.5 V supply voltage operation
2. A spintronic transistor with less than 500 nm channel length
3. Metal nanocrystal and floating gate flash memory
4. GaN based high electron mobility transistors
5. New generation printable organic semiconductors based on conjugated polythiophenes
6. Nano-Electro-Mechanical Systems for sensing applications
Joint Deliverables with IISc

1. A microfluidic flow cytometer chip with integrated optical system
2. An integrated soil moisture, temperature and air humidity sensor with on-board electronics
Available Infrastructure

- State of the art cleanrooms at IITB and IISc
- An excellent fab facility to support networked activities
- Characterization facilities
- Dedicated support staff
Education & HRD in CENs

- PhD: ~70 graduates per year, total over 5 years: 350
- MS: 86 graduates per year, total over 5 years: 430
- BTech: 36 graduates per year, total over 5 years: 180
- Staff: 38 graduates per year, total over 5 years: 190
- Postdocs: 9 graduates per year, total over 5 years: 45
Technology Development & Incubation
Application Development

- Clear focus on technology applications
- Continuous interaction with industries & users
- Thrust on prototyping for devices and systems
- Thrust on technology IP generation
Projects: about 7%
Consumables (6%) + part of manpower (4%)
CEN Phase II Budget

US $ 30 M
Projects ~ 40%
Consumables (21%) + part of manpower (18%)
Different Modes of Industry Interaction

- Establishment of Endowed (Named) Laboratories
- Equipment donation
- Sponsored projects
- Consultancy
- Sponsorship for Graduate Students*
- Usage of INUP Facilities
- Internships for students
Thank You