Plasma Immersion Ion Implantation (PIII)

As CMOS device gate length has shrunk to 45nm, the short channel effects (SCE) become very severe. To reduce SCE one of the solution is to make very shallow S/D junctions. For the same, we require implant energy less than 2KeV, where commercial Ion Beam Implanters have several issues like beam current instabilities at low voltages.
PIII is very suitable for ion energy even at 200V operation. This system uses BF3 and PH3 gasses for Boron (p-type) and Phosphorus (n-type) implants in Si wafers.

Make and Model: ***This system has been build at IITB with help of Excel Instruments.***

Specifications:

- ICP source SENTECH PTSA 200 (0-1200W, 13.56MHz).
- High voltage (-5 to 0V) negative bias applied to grid.
- Wafer placed on 10" chuck which is grounded.

Process Capabilities:

- **Type of Implants:** Phosphorus and Boron.
- **Types of substrates:** 2" – 8" Si wafers, small pieces of wafers.
- **Gases used:** PH3, BF3
- **Substrate History:** substrates having any metal or organic should be avoided.
- **Load lock chamber base pressure**: 1e-6 mbar
- **Process chamber base pressure**: 1e-6mbar